Appl. No. 10/694,155
Examiner: CHEN, JACK S J, Art Unit 2813
In response to the Office Action dated December 6, 2004

Date: March 5, 2005
Attorney Docket No. 10110752

AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph beginning on page 3, line 8 with the following rewritten paragraph:

-- According to one aspect, the invention provides a method for fabricating a vertical NROM cell. First, a substrate having at least one trench is provided. A spacer is formed over the sidewall of the trench. Subsequently, ion implantation is performed in the substrate using the spacer as a mask to form doping areas as bit lines in the substrate near its surface and the bottom of the trench. Bit line oxides are formed over each of the doping areas. After the spacer is removed, a conformable insulating layer as gate dielectric is deposited on and in direct contact with the substrate surface that constitutes the sidewalls ~~the sidewall~~ of the trench and the surface of the bit line oxide. Finally, a conductive layer as a word line is deposited over the insulating layer and fills in the trench.

Please replace the paragraph beginning on page 3, line 21 with the following rewritten paragraph:

-- According to another aspect, the invention provides a vertical NROM cell. The memory cell includes a substrate having at least one trench, bit lines, bit line oxides, a gate dielectric layer, and a word line. The bit lines are formed in the substrate near its surface and the bottom of the trench. Each of the bit line oxides is disposed over each of the bit lines. The gate dielectric layer is conformably formed on and in direct contact with the substrate surface that constitutes the sidewalls ~~the sidewall~~ of the trench and the surface of the bit line oxide. The word line is disposed over the gate dielectric layer and fills in the trench.